ABSTRACT

QUADRATURE AMPLITUDE MODULATION DEMODULATOR AND RECEIVER

A QAM demodulator comprises a timing synchroniser whose output is supplied via an adaptive equaliser to a carrier synchroniser, all of which are controlled by a controller. The timing synchroniser resamples the incoming signal in the digital domain with a sampling period which, during an acquisition mode, sweeps between limit values at different rates. The controller begins an acquisition cycle at the highest rate and monotonically lowers the sweep rate until timing lock is achieved. The sampling rate is then fixed at the correct value. Similarly, the controller sweeps the local oscillator of a phase locked loop in the carrier synchroniser initially at a highest rate and at progressively lower rates until the carrier synchroniser locks to the phase of the incoming signal.

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